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FPGA Based IP Core Initialization for Ps2-Vga Peripherals Using Microblaze Processor

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Abstract
The MICROBLAZE processor is a soft core microprocessor that is used in FPGA with Xilinx EDK (embedded development kit) tool. Embedded Development Kit (EDK) is a suite of tools and Intellectual Property (IP) that enables you to design a complete embedded processor system for implementation in a Xilinx Field Programmable Gate Array (FPGA) device. Xilinx Platform Studio (XPS) is the development environment used for designing the hardware portion of your embedded processor system based on MICROBLAZE.
In this paper the ps2-vga peripherals IP cores are initialized and provided an embedded environment under MICROBLAZE processor using Xilinx Platform Studio (XPS).

I. INTRODUCTION

The MICROBLAZE embedded soft core is a reduced instruction set computer (RISC) optimized for implementation in Xilinx Field programmable gate arrays (FPGAs). The MICROBLAZE has a versatile interconnect system to support a variety of embedded applications. MICROBLAZE'S primary I/O bus, the core connect PLB bus, is a traditional system-memory mapped transaction bus with master/slave capability. The MICROBLAZE processor is a 32-bit Harvard Reduced Instruction Set Computer (RISC architecture optimized for implementation in Xilinx FPGAs with separate 32-bit instruction and data buses running at full speed to execute programs and access data from both on-chip and external memory at the same time. The backbone of the architecture is a single-issue, 3-stage pipeline with 32 general-purpose registers (does not have any address registers like the Motorola 68000 Processor), an Arithmetic Logic Unit (ALU), a shift unit, and two levels of interrupt. This basic design can then be configured with more advanced features to tailor to the exact needs of the target embedded application such as: barrel shifter, divider, multiplier, single precision floating-point unit (FPU), instruction and data Caches, exception handling, debug logic, Fast Simplex Link (FSL) interfaces and others. This flexibility allows the user to balance the required performance of the target application against the logic area cost of the soft processor. Figure 1 shows a View of a MICROBLAZE system. The items in white are the backbone of the MICROBLAZE architecture while the items shaded gray are optional features available depending on the exact needs of the target embedded application. Because MICROBLAZE is a soft-core microprocessor, any optional features not used will not be implemented and will not take up any of the FPGAs resources.

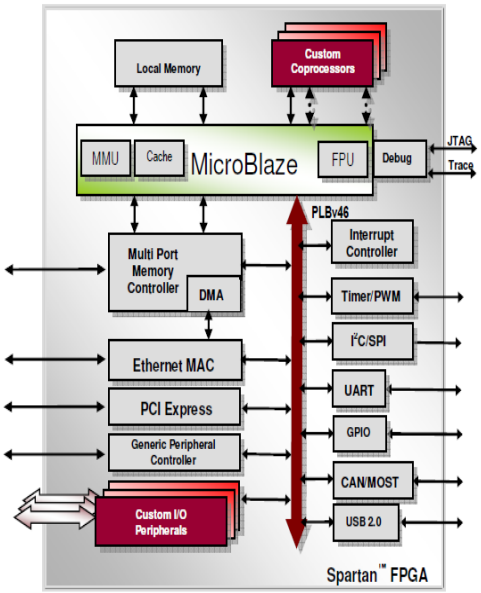

Fig1. MICROBLAZE processor architecture

The MICROBLAZE processor is useless by itself without some type of peripheral devices to connect to and EDK comes with a large number of commonly used peripherals. Here we are using PS2 and VGA peripherals to develop the application in EDK-XPS using MICROBLAZE processor in SPARTAN 3E starter board**.**

II. PS2 PRIPHERAL

The Spartan-3E FPGA Starter Kit board includes a PS/2 mouse/keyboard port and the standard 6-pin mini-DIN connector, labeled J14 on the board. Only pins 1 and 5 of the connector attach to the FPGA.

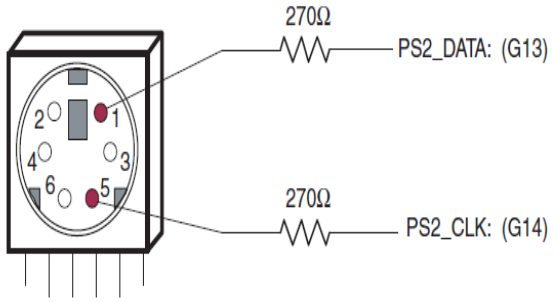

Fig 2 . PS2 connector

Both a PC mouse and keyboard use the two-wire PS/2 serial bus to communicate with a host device, the Spartan-3E FPGA in this case. The PS/2 bus includes both clock and data. Both a mouse and keyboard drive the bus with identical signal timings and both use 11-bit words that include a start, stop and odd parity bit. However, the data packets are organized differently for a mouse and keyboard. Furthermore, the keyboard interface allows bidirectional data transfers so the host device can illuminate state LEDs on the keyboard.

PS/2 DIN Pin	Signal	FPGA Pin
1	DATA (PS2_DATA)	G13
2	Reserved	G13
3	GND	GND
4	+5V	–
5	CLK (PS2_CLK)	G14
6	Reserved	G13

Fig 3. PS2 connector pinout

The keyboard uses open-collector drivers so that either the keyboard or the host can drive the two-wire bus. If the host never sends data to the keyboard, then the host can use simple input pins. A PS/2-style keyboard uses scan codes to communicate key press data. Nearly all keyboards in use today are PS/2 style. Each key has a single, unique scan code that is sent whenever the corresponding key is pressed. If the key is pressed and held, the keyboard repeatedly sends the scan code every 100 ms or so. When a key is released, the keyboard sends an "F0" key-up code, followed by the scan code of the released key. The keyboard sends the same scan code, regardless if a key has different shift and non-shift characters and regardless whether the Shift key is pressed or not. The host determines which character is intended.

Some keys, called extended keys, send an "E0" ahead of the scan code and furthermore, they might send more than one scan code. When an extended key is released, an "E0 F0" key-up code is sent, followed by the scan code. The keyboard sends commands or data to the host only when both the data and clock lines are High, the Idle state. Because the host is the bus master, the keyboard checks whether the host is sending data before driving the bus. The clock line can be used as a clear to send signal. If the host pulls the clock line Low, the keyboard must not send any data until the clock is released.

III. VGA PERIPHERAL

The Spartan 3E FPGA Starter Kit board includes a VGA display port via a DB15 connector. Connect this port directly to most PC monitors or flat-panel LCDs using a standard monitor cable. The below figure shows VGA connector.

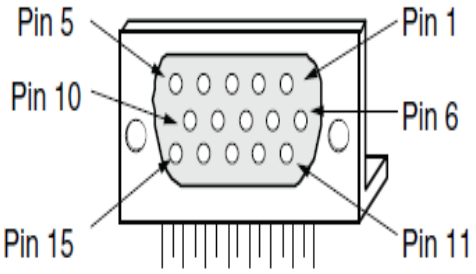

Fig 4. VGA connector

The Spartan-3E FPGA directly drives the five VGA signals via resistors. Each color line has a series resistor, with one bit each for VGA_RED, VGA_GREEN, and VGA_BLUE.

The VGA_HSYNC and VGA_VSYNC signals using LVTTL or LVCMOS33 I/O standard drive levels. The VGA controller generates the horizontal sync (HS) and vertical sync (VS) timings signals and coordinates the delivery of video data on each pixel clock. The pixel clock defines the time available to display one pixel of information. The VS signal defines the refresh frequency of the display, or the frequency at which all information on the display is redrawn. The number of horizontal lines displayed at a given refresh frequency defines the horizontal retrace frequency.

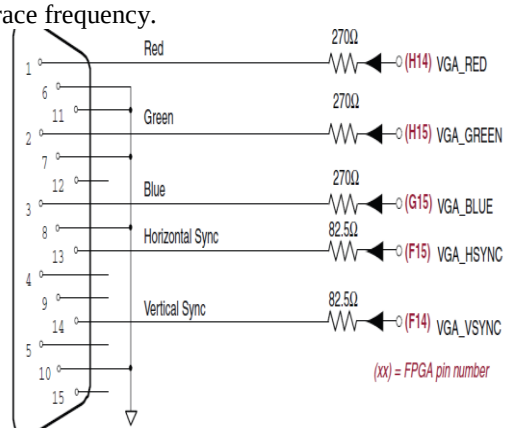

Fig 5 . VGA connections from spartan 3e starter kit

Drive the VGA_RED, VGA_GREEN, and VGA_BLUE signals High or Low to generate the eight colors shown below

VGA_RED	VGA_GREEN	VGA_BLUE	Resulting Color
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

Fig 6. 3 bit binary color codes

IV. IMPLEMENTATION AND EXPERIMENTAL RESULTS

A. PS2-VGA initialization using XPS

XPS-PS2 is the IP core that is provided by XILINX plat form studio after creating a sample project. Xps_ps2 is added by selecting IP catalog tab in project information tab in XPS. The selected IP core will appear in bus interface tab of system assembly view. The ps2 controller will be connected to mb_plb i.e. the processor local bus connection in order to perform communication with MICROBLAZE processor.

Vga_0 custom IP core created using create or import peripheral wizard in XPS. The "Create/Import Peripheral Wizard" in the Xilinx Embedded Development Kit (EDK) assists increasing a custom peripheral that is accessible from a MICROBLAZE processor.

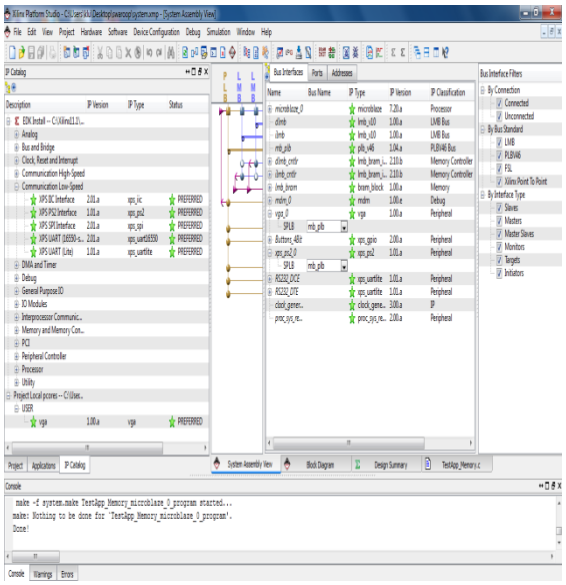

Fig7. IP core creation for PS2 & VGA peripherals

B. Making PS2-VGA ports externals

After the initialization of PS2-VGA IP cores the respective ports must be made external. After making the external the ports of the peripherals connected to the MICROBLAZE processer local bus.

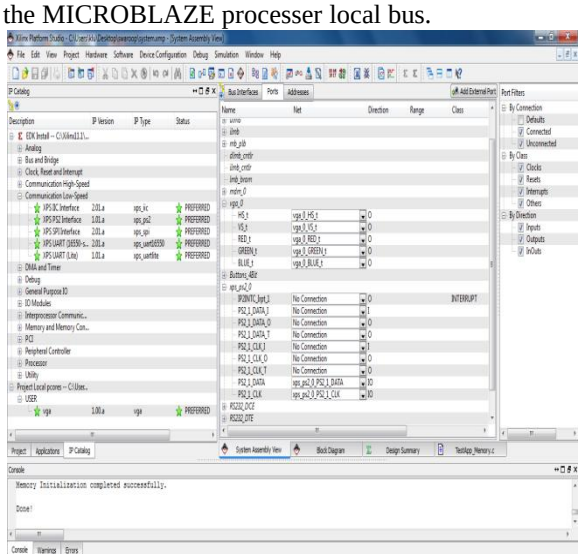

Fig8 . PS2-VGA ports are made external

C. Adress generation

After making the ports externals of these two peripherals the adress will generate at adress tab in system assemly view. It gives the base adress and high adress for thse both PS2 and VGA peripherals.

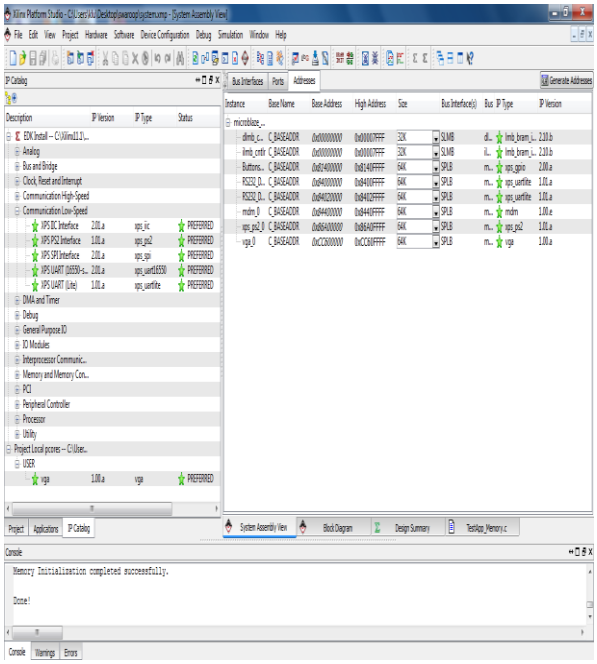

Fig9 . Adress generated for PS2-VGA peripherals

After the adress genaration MHS (Microprocessor hardware specification) and MPD(Microprocessor peripheral descripton) must be edit depends upon peripheral device configuration. The UCF(user constraint file) must be given at the system.ucf in project information tab.

After intialization of these two peripherals, PS/2 keyboard scan code receiving and processing

program, the other one is VGA displaying program. The applications will run on XPS using Xilinx-"c".

V. CONCLUSION

The Xilinx platform studio under MICROBLAZE processor is used to design embedded processor to develop applications with peripheral devices using fpga. Some files are written depends upon the peripheral configuration and specifications those are MHS,MPD,MSS and UCF to develop the interface between peripherals and intilization. We can run any of the application which is working through PS2-VGA peripherals.

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